REMARKS

Claims 9-39 are pending, with claims 9, 18, 19, 28 and 33 being independent. Claims 9 and 18 have been amended.

Claims 9, 10-17, 29 and 35 have been provisionally rejected for obviousness-type double patenting in view of claim 8 of the '282 application. Applicants request reconsideration and withdrawal of this rejection because, as conceded by the Examiner, claim 8 of the '282 application does not include using the first electrode as a mask to form a high concentration impurity region or adding an impurity element to the semiconductor layer using the second conductive layer as a mask to form a low concentration impurity region, as recited in claim 9. The action relies upon paragraph 40 of the '282 application as describing these steps, and relies upon the specification of the '282 application as describing the subject matter of the dependent claims. Such reliance is improper. See MPEP 804.

Claims 18, 19, 20-27, 30, 31, 36 and 37 have been provisionally rejected for obviousness-type double patenting in view of claim 10 of the '334 application. With respect to claims 18 and 19, applicants will consider whether to file a terminal disclaimer when the claims are otherwise found to be allowable. With respect to dependent claims 20-27, 30, 31, 36 and 37, applicants note that the action relies upon the specification of the '334 application as describing the subject matter of these claims, which, as noted above, is improper.

Finally, the action indicates that claims 28 and 33 would be allowable if rewritten to overcome the rejection under section 112, second paragraph. However, no such rejection appears in the action.

Applicants request allowance of all of the claims.

Attached is a marked-up version of the changes being made by the current amendment.

Enclosed is a $410 check for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: March 20, 2003

John F. Hayden
Reg. No. 37,640

Fish & Richardson P.C.
1425 K Street, N.W.
11th Floor
Washington, DC 20005-3500
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

40146137.doc

Version with markings to show changes made

In the claims:

Claims 9 and 18 have been amended as follows:

9. (Amended) A method of manufacturing a semiconductor device comprising steps of:

forming a semiconductor layer on an insulating surface;

forming an insulating film on said semiconductor layer;

forming a first electrode comprising a laminate structure of a first conductive layer with a first width and a second conductive layer on said insulating film;

adding an impurity element to said semiconductor layer using said first electrode as a mask to form a high concentration impurity region;

etching said second conductive layer to form a second electrode comprising a laminate structure of the first conductive layer with said first width and said second conductive layer with a second width;

adding the impurity element to said semiconductor layer using said second conductive layer as a mask to form a low concentration impurity region; and

after forming the low concentration impurity region, etching said first conductive layer to form a third electrode comprising a laminate structure of said first conductive layer with a third width and said second conductive layer with said second width.

18. (Amended) A method of manufacturing a semiconductor device comprising steps of:

forming a semiconductor layer on an insulating surface;

forming an insulating film on said semiconductor layer;

forming a first electrode comprising a laminate structure of a first conductive layer with a first width and a second conductive layer on said insulating film;

etching said second conductive layer to form a second electrode comprising a laminate structure of said first conductive layer with said first width and said second conductive layer with a second width;

adding an impurity element to said semiconductor layer using said second electrode as a mask to form a high concentration impurity region;

adding said impurity element to said semiconductor layer of the second electrode through said first conductive layer of the second electrode using the second conductive layer as a mask to form a low concentration impurity region; and

etching said first conductive layer to form a third electrode comprising a laminate structure of said first conductive layer with a third width and said second conductive layer with said second width.